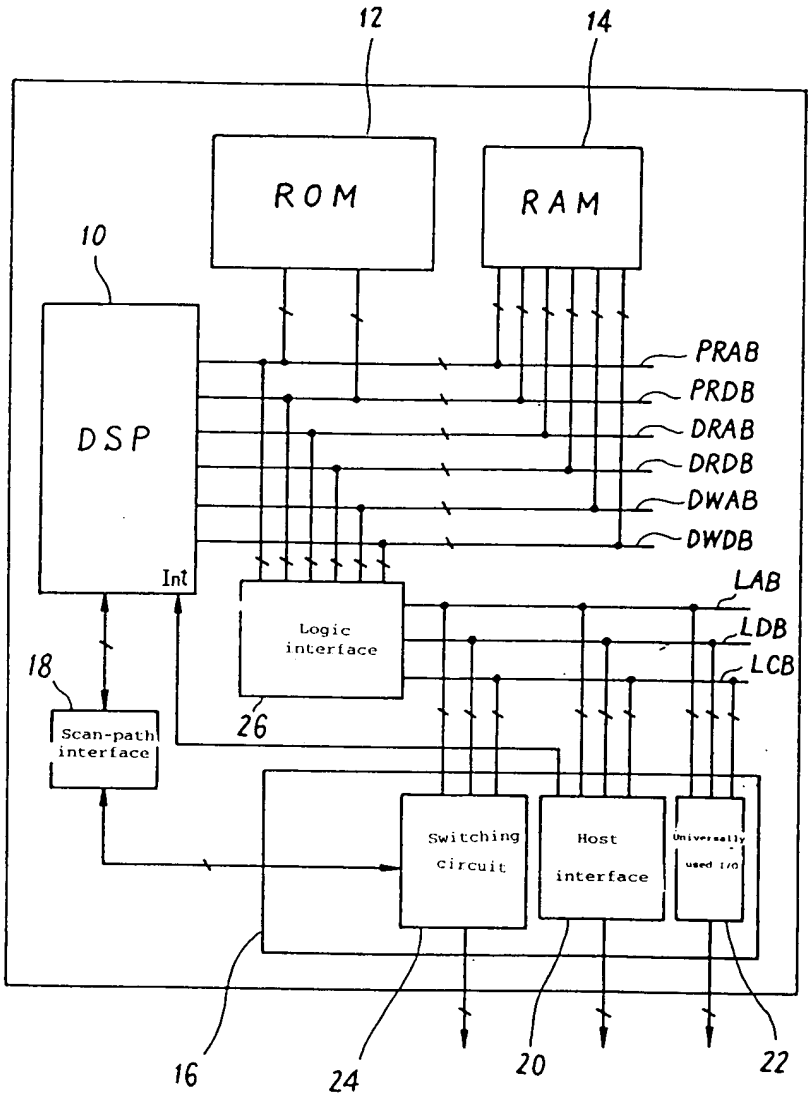
12
14
ROM
RAM
10
DSP
Int
PRAB
PRDB
DRAB
DRDB
DWAB
DWDB
LAB
LDB
LCB
Logic interface
18
Scan-path interface
26
Switching circuit
Host interface
Universally used I/O
16
24
20
22

FIG. 1

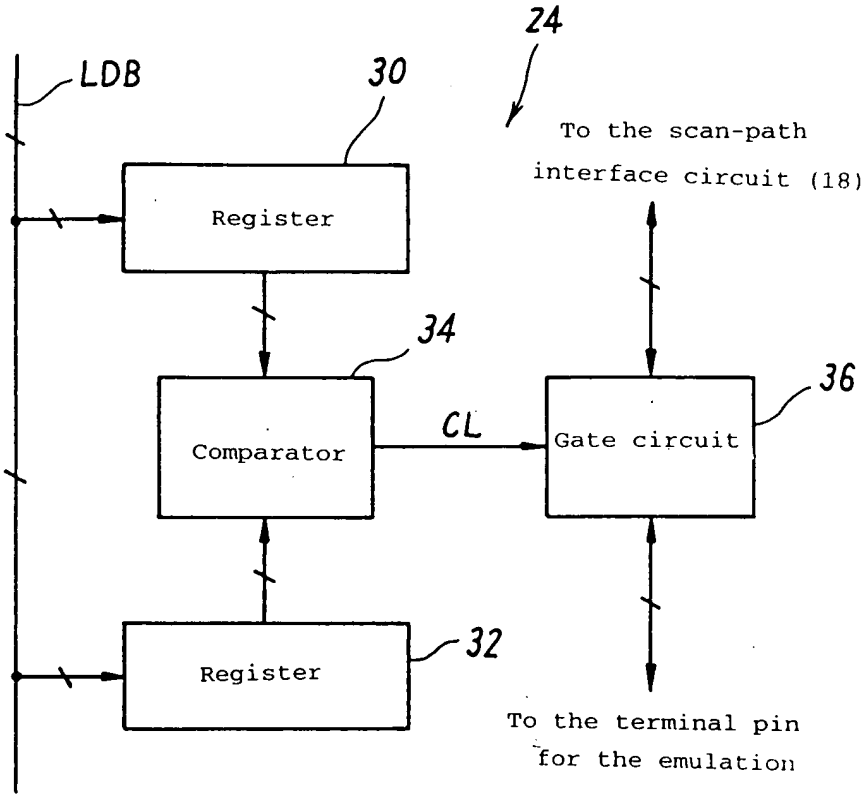
24
LDB
30
To the scan-path
interface circuit (18)
Register
34
36
Comparator
CL
Gate circuit
Register
32
To the terminal pin
for the emulation

FIG. 2

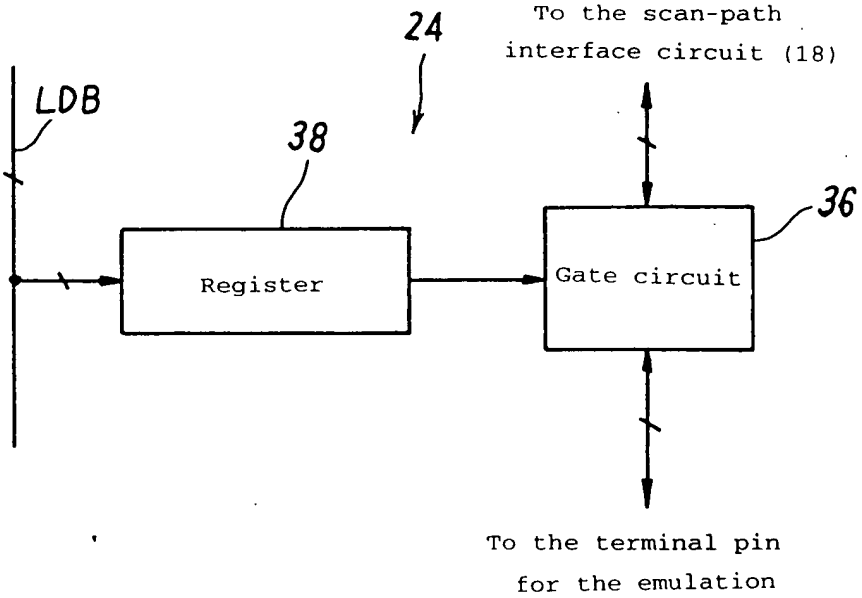
24
To the scan-path
interface circuit (18)
LDB
38
36
Register
Gate circuit
To the terminal pin
for the emulation

FIG. 3

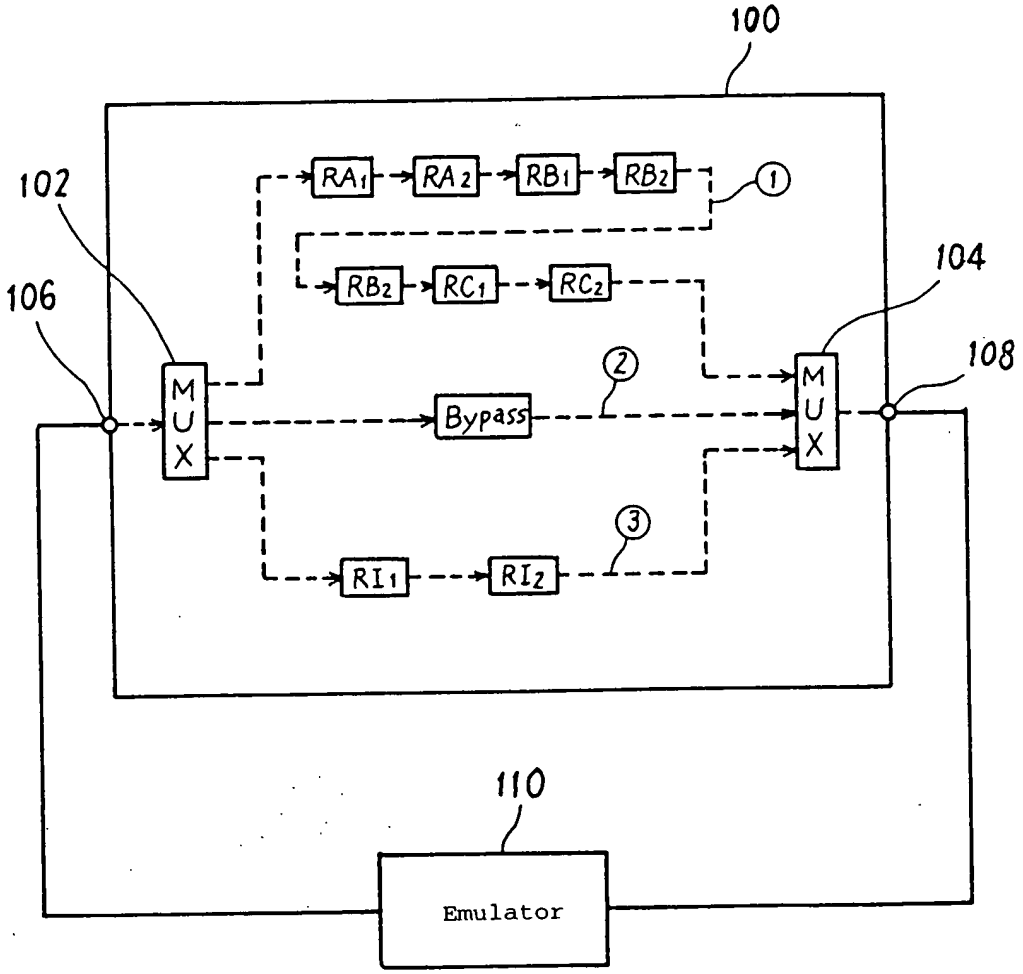
100
102
104
106
108
110
RA1
RA2
RB1
RB2
RB2
RC1
RC2
RI1
RI2
Bypass
MUX
MUX
Emulator
1
2
3

FIG. 4